WHAT IS CLAIMED IS:

1. A digital system, comprising:

a bridge;

a first bus coupled to the bridge;

a clock generator;

a first multiplexer coupled to the clock generator, the first bus, and the bridge; wherein the first multiplexer is configured to pass one of a first clock signal from the clock generator and a second clock signal from the bridge to the first bus.

2. The digital system of claim 1, wherein the bridge is coupled to the clock generator and configured to receive from the clock generator a third clock signal which is in phase with and at a same frequency as the first clock signal.

3. The digital system of claim 2, wherein the bridge comprises a bus logic coupled to the clock generator and the first bus, wherein the bus logic is configured to receive the third clock signal and operate based on the third clock signal.

4. The digital system of claim 2, wherein the first multiplexer is further configured to receive a select signal from the bridge and pass one of the first clock signal and the second clock signal to the first bus based on the select signal.

5. The digital system of claim 4, further comprising at least two adapters coupled to the first bus, wherein the bridge is further configured to generate the second clock signal to the first multiplexer, and cause the first multiplexer to pass one of the first clock signal and the second clock signal to the first bus based on a speed of a slowest adapter on the first bus.

6. The digital system of claim 5, wherein the second clock signal is at one of at least a first frequency and a second frequency, the first frequency being different than the second frequency.

7. The digital system of claim 6, further comprising:

a second bus coupled to the bridge;

a second multiplexer coupled to the clock generator, the second bus, and the bridge; wherein the second multiplexer is configured to pass one of a fourth clock signal from the clock generator and a fifth clock signal from the bridge to the second bus.

8. The digital system of claim 1, further comprising:

a second bus coupled to the bridge;

a second multiplexer coupled to the clock generator, the second bus, and the bridge; wherein the second multiplexer is configured to pass one of a third clock signal from the clock generator and a fourth clock signal from the bridge to the second bus.

9. The digital system of claim 8, further comprising at least two adapters coupled to the second bus, wherein the bridge is further configured to generate the fourth clock signal to the second multiplexer, and cause the second multiplexer to pass one of the third clock signal and the fourth clock signal to the second bus based on a speed of a slowest adapter on the second bus.

10. The digital system of claim 9, wherein the third clock signal is in phase with and at a same frequency as the first clock signal.

11. The digital system of claim 10, wherein the fourth clock signal is at one of at least the first frequency and the second frequency.

12. A method for clock generation in a digital system, the method comprising:

providing a first bus coupled to a bridge and a first multiplexer coupled to a clock generator, the first bus, and the bridge; and

passing, by operation of the first multiplexer, one of a first clock signal from the clock generator and a second clock signal from the bridge to the first bus.

13. The method of claim 12, further comprising generating, with the clock generator, a third clock signal to the bridge, the third clock signal being in phase with and at a same frequency as the first clock signal.

14. The method of claim 13, wherein the step of passing, by the operation of the first multiplexer, one of a first clock signal from the clock generator and a second clock signal from the bridge to the first bus comprises:

applying a select signal from the bridge to the first multiplexer; and

passing, by operation of the first multiplexer, one of the first clock signal and the second clock signal to the first bus based on the select signal.

15. The method of claim 14 further comprising:

providing at least two adapters coupled to the first bus;

generating, with the bridge, the second clock signal to the first multiplexer; and

passing, by operation of the first multiplexer, one of the first clock signal and the second clock signal to the first bus based on a speed of a slowest adapter on the first bus.

16. The method of claim 15, wherein the step of generating, with the bridge, the second clock signal to the first multiplexer comprises generating, with the bridge, the second clock signal at one of at least a first frequency and a second frequency, the first frequency being different than the second frequency.

17. The method of claim 16, further comprising:

providing a second bus coupled to the bridge;

providing a second multiplexer coupled to the clock generator, the second bus, and the bridge; and

passing, by the operation of the second multiplexer, one of a fourth clock signal from the clock generator and a fifth clock signal from the bridge to the second bus.

18. The method of claim 12, further comprising:

providing a second bus coupled to the bridge;

providing a second multiplexer coupled to the clock generator, the second bus, and the bridge; and

passing, by the operation of the second multiplexer, one of a third clock signal from the clock generator and a fourth clock signal from the bridge to the second bus.

19. The method of claim 18, further comprising:

providing at least two adapters coupled to the second bus;

generating, with the bridge, the fourth clock signal to the first multiplexer; and

passing, by the operation of the second multiplexer, one of the third clock signal and the fourth clock signal to the second bus based on a speed of a slowest adapter on the second bus.

20. The method of claim 19, wherein the third clock signal is in phase with and at a same frequency as the first clock signal.

21. The method of claim 20, wherein the step of generating, with the bridge, the fourth clock signal to the second multiplexer comprises generating, with the bridge, the fourth clock signal at one of at least a first frequency and a second frequency, the first frequency being different than the second frequency.

22. A digital system, comprising:

a bridge;

N buses coupled to the bridge;

a clock generator; and

N multiplexers each of which is coupled to the clock generator, the bridge, and one of the N buses, one on one; wherein each of the N multiplexers is configured to pass one of a first clock signal from the clock generator and a second clock signal from the bridge to the respective bus.

23. The digital system of claim 22, wherein each of the N buses is one of a secondary PCI bus and a secondary PCI-X bus.

24. The digital system of claim 22, wherein the bridge comprises a PLL circuit which is configured to receive a third clock signal from the clock generator which is in phase with and at a same frequency as the first clock signal.

25. The digital system of claim 24 wherein the bridge further comprises N bus logics coupled to the PLL circuit and to the N buses, one to one, wherein each of the N bus logics is configured to receive a fourth clock signal from the PLL circuit and operate based on the fourth clock signal.